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Digital & Photonic Test Division
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Agilent Technologies



M8000 Series of BER Test Solutions

Take the Express Lane
to Design Verification

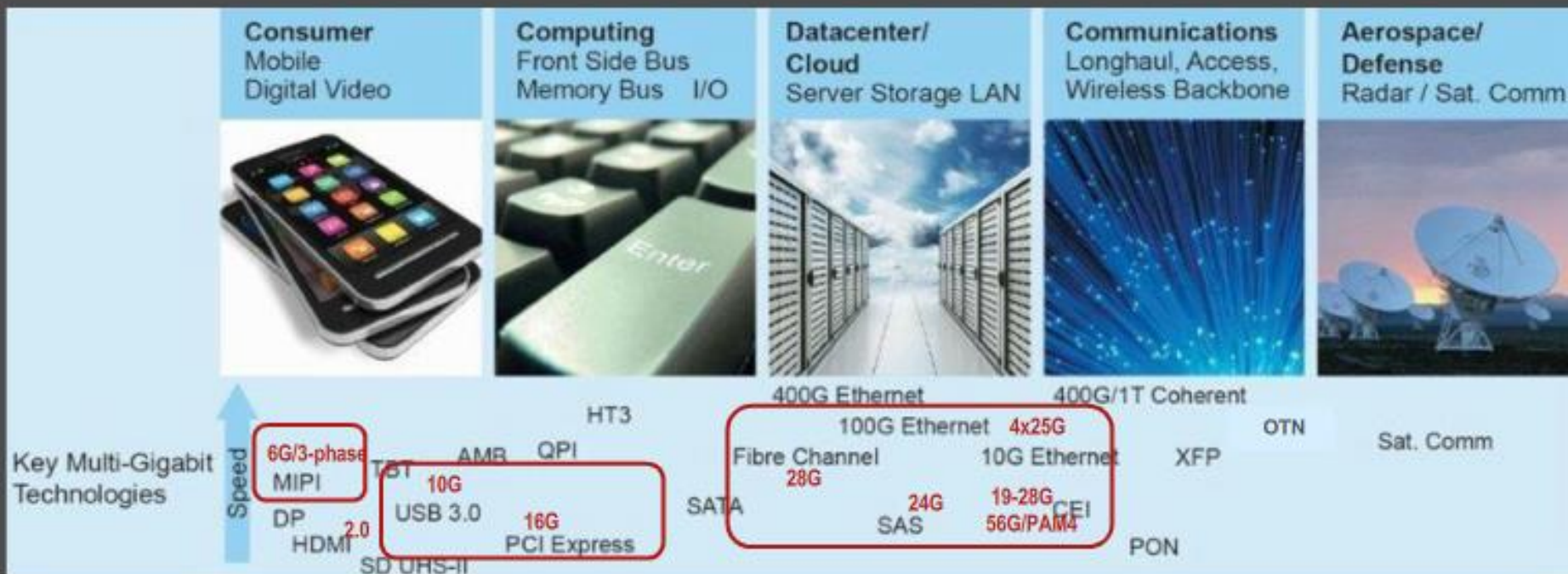
Michael Reser

Sales and Business Development
Manager



High-Speed Digital Markets & Technologies

2014/15 Hot Technologies for BER Test solutions



Hot spots for BERTs in 2014/2015:

- **“Generation 4”** computer buses coming (PCIe 4, USB3 10G)
- Investments shift towards **mobile** computing (MIPI)
- Web traffic increase drives **datacenter** build-out (100GbE)



High-speed Digital I/Os

The Customer's Challenge:

R&D and test engineers need to characterize the next generation of mobile, computer and networking devices. Designs for higher bandwidths, less spaces and less power. Time pressure increases. RX test becomes more and more complicated and mandatory.



Mobile MIPI

- M-PHY: 6G/12G (gear3/4)
- Multi-lane, skew, PWM
- D-PHY (3G)
- 3-phase signaling
- Many versions – always a custom RX solution
- Built-in error counters



Gen 4 Computing

- PCIe4 (16G), USB3.1 (10G)
- Link training
- 128/130 or 128/132 coding
- Stress calibration at TP
- TX De-emphasis and RX equalization
- Interference



Datacenter

- 10GbE ports at server CPUs
- Many 100GbE (4x 25G), 32G FC, CEI (28/56G)
- Electrical + optical
- Crosstalk
- PAM4 and higher modulation formats



Transition to M8000 Series

*Highly integrated
and scalable for simplified,
time efficient testing*



J-BERT N4903A, 1 channel

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J-BERT N4903A, 1 channel



ParBERT, multi-channel

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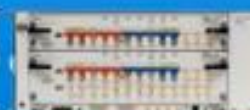
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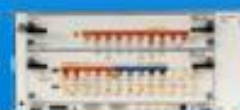
M8000 Series of BER Test Solutions



16 Gbit J-BERT M8020A
1 - 2 channel



16 Gbit J-BERT M8020A
4 channel



32 Gbit J-BERT M8020A
and M8051A, 1 channel



M8190A AWG,
2 channel



J-BERT N4903A, 1 channel



ParBERT, multi-channel

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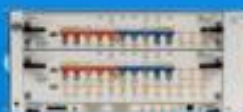
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and M8051A, 1 channel



M8190A AWG,
2 channel

 Higher integration: CDR, de-emphasis



J-BERT N4903A, 1 channel



ParBERT, multi-channel

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1 - 2 channel



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32 Gb/s J-BERT M8020A
and M8051A, 1 channel



M8190A AWG,
2 channel

☞ Expandable to higher data rates up to 32 Gb/s

☞ Higher integration: CDR, de-emphasis



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16 Gb/s J-BERT M8020A
1 + 2 channel



16 Gb/s J-BERT M8020A
4 channel



32 Gb/s J-BERT M8020A
and M8051A, 1 channel



M8190A AWG,
2 channel

☞ Stress calibration at test point, de-embedding

☞ Expandable to higher data rates up to 32 Gb/s

☞ Higher integration: CDR, de-emphasis



J-BERT N4903A, 1 channel



ParBERT, multi-channel

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16 Gb/s J-BERT M8020A
1 - 2 channel



16 Gb/s J-BERT M8020A
4 channel



32 Gb/s J-BERT M8020A
and M8001A, 1 channel



M8190A AWG,
2 channel

☞ Analyzer equalization

☞ Stress calibration at test point, de-embedding

☞ Expandable to higher data rates up to 32 Gb/s

☞ Higher integration: CDR, de-emphasis



J-BERT N4903A, 1 channel



ParBERT, multi-channel

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16 Gbit J-BERT M8020A
4 channel



32 Gbit J-BERT M8020A
and M8001A, 1 channel



M8100A AWG,
2 channel

☞ Interactive link training

☞ Analyzer equalization

☞ Stress calibration at test point, de-embedding

☞ Expandable to higher data rates up to 32 Gb/s

☞ Higher integration: CDR, de-emphasis



J-BERT N4903A, 1 channel



ParBERT, multi-channel

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M8000 Industry Leading Performance

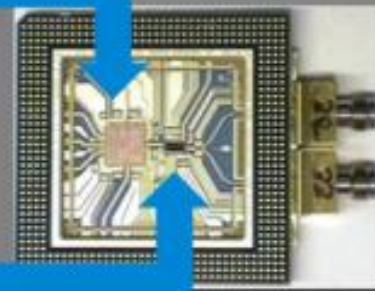
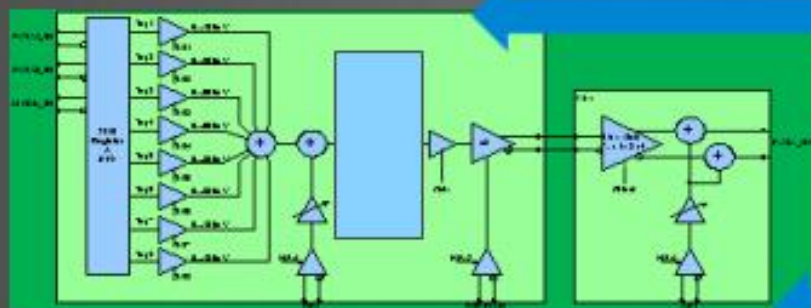
Highest integration for robust and reliable testing

J-BERT M8020A 16G and 32G



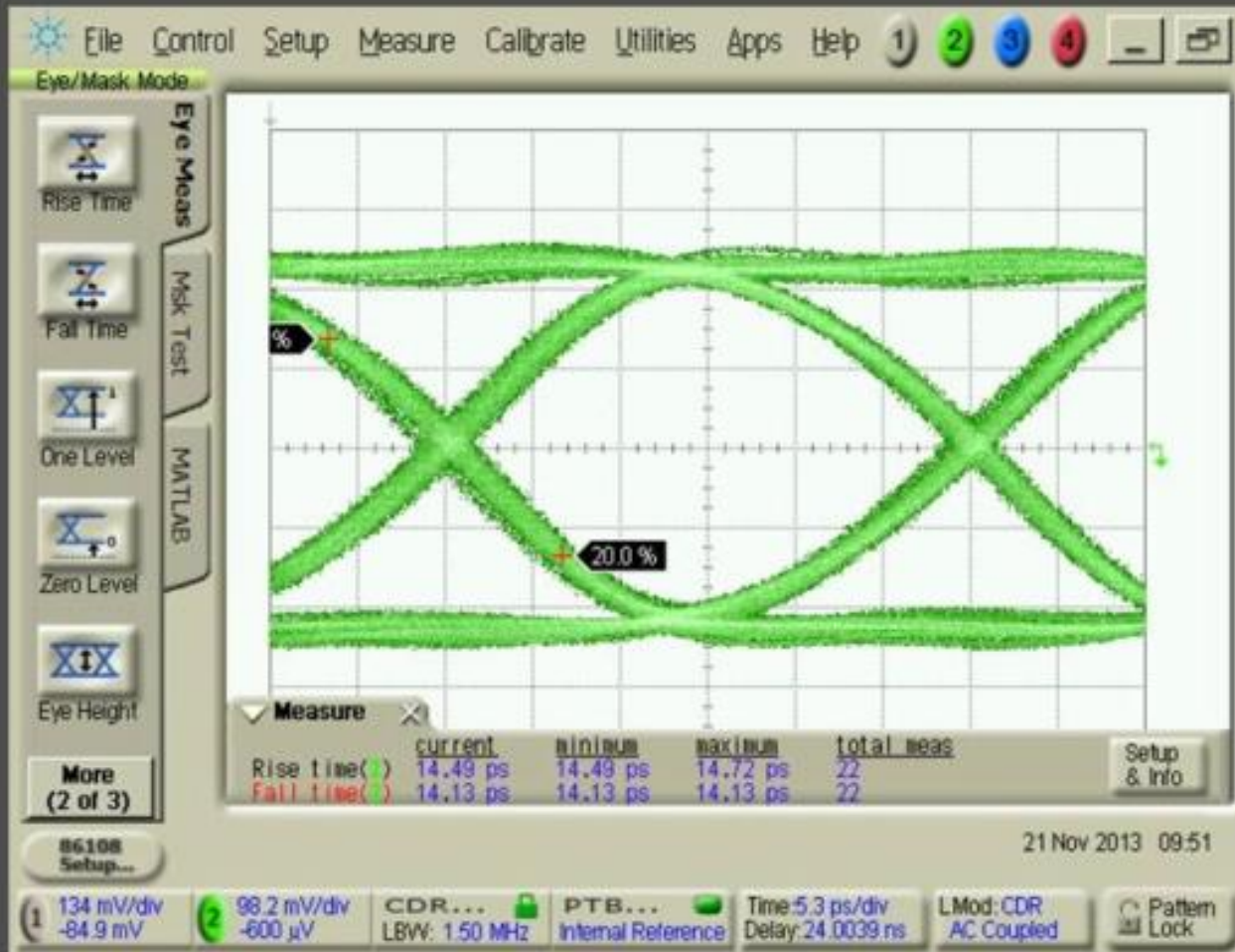
pre amplifier

post amplifier



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J-BERT M8020A 32 Gb/s Excellent Eye Performance



For accurate and repeatable results:

- Clean eyes with lowest intrinsic jitter
- Fast transitions
- Calibrated jitter sources and Clk/2
- Internal superposition of interference
- 8-tap de-emphasis, positive/negative
- For electrical and optical interfaces

Measured with DCA-X 86108B at M8061A output: PRBS7, w/o BPF and with internal clock from M8041A



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Ultra-low Intrinsic Jitter - M8061A Output



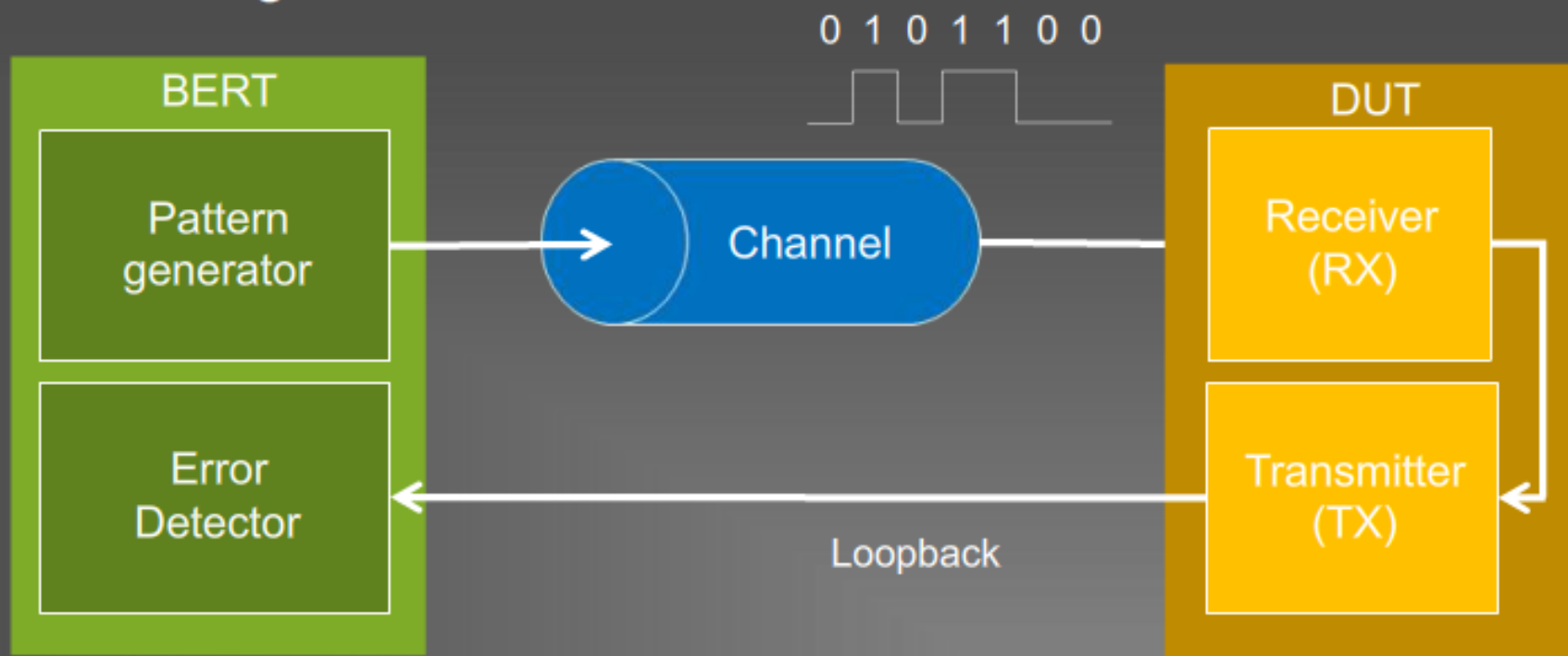
Ultra-clean electrical eyes at M8061A output with optimized intrinsic jitter performance (150 fs rms)

Preliminary. Measured with DCA-X 86108B at M8061A output: clock pattern, 1 Vpp differential, jitter sources on/0 mUI

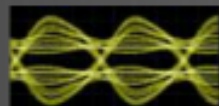


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Generating RX Stress Conditions



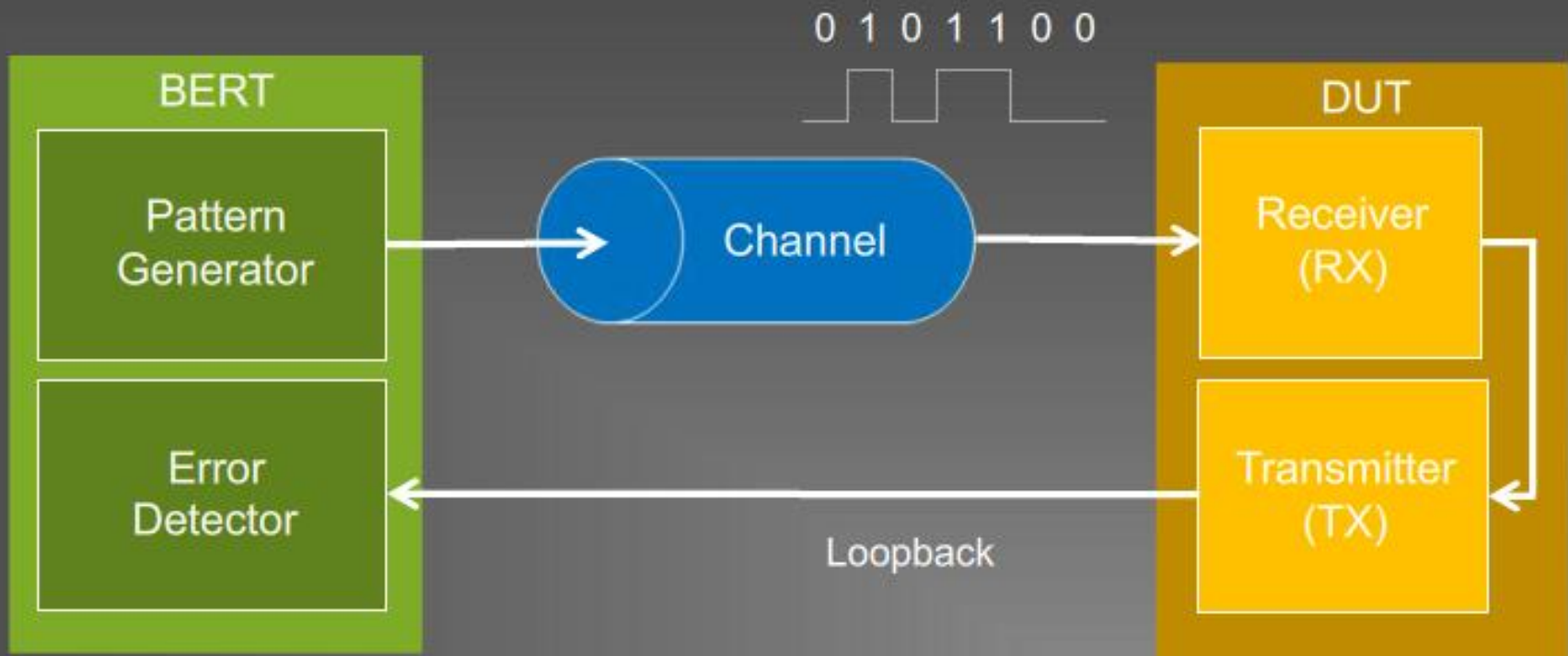
The BERT pattern generator provides adjustable and repeatable stress conditions to verify the RX tolerance margins in the most accurate way:



- 8-tap de-emphasis
- jitter, interference, channel loss
- X-talk and skew for multi-lane interfaces
- lock to a system reference clock
- emulate channel ISI



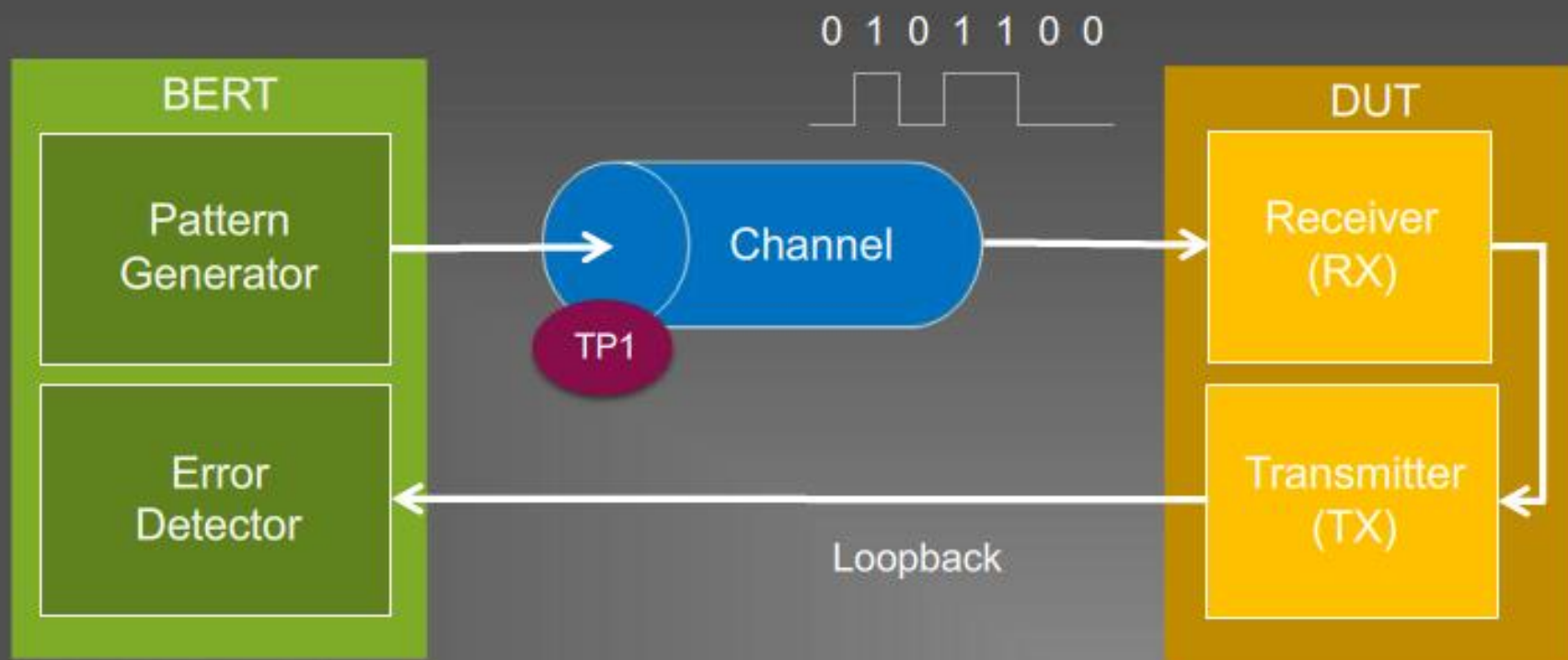
In-situ Calibration for Accurate and Repeatable Results



- Calibration test point (TP) moves closer to RX
- Compensate for the channel loss, ISI and the test setup



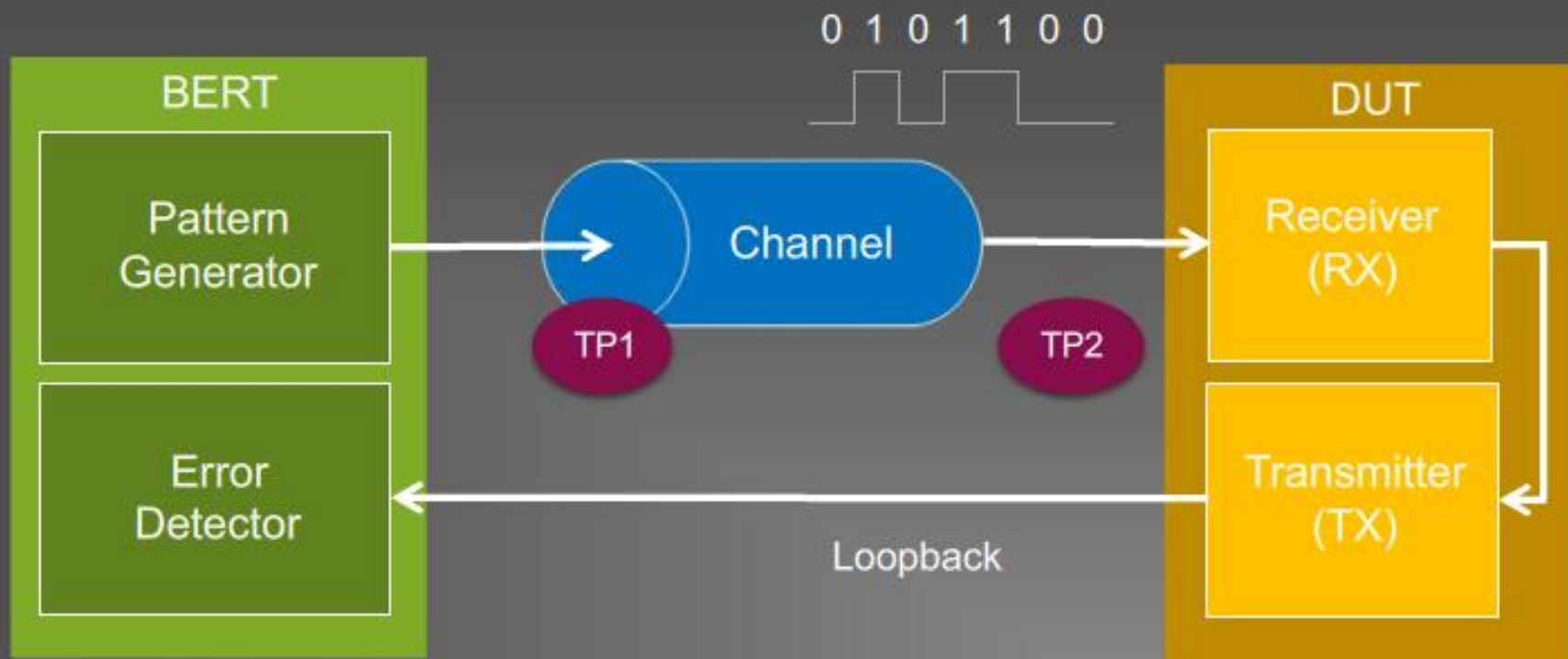
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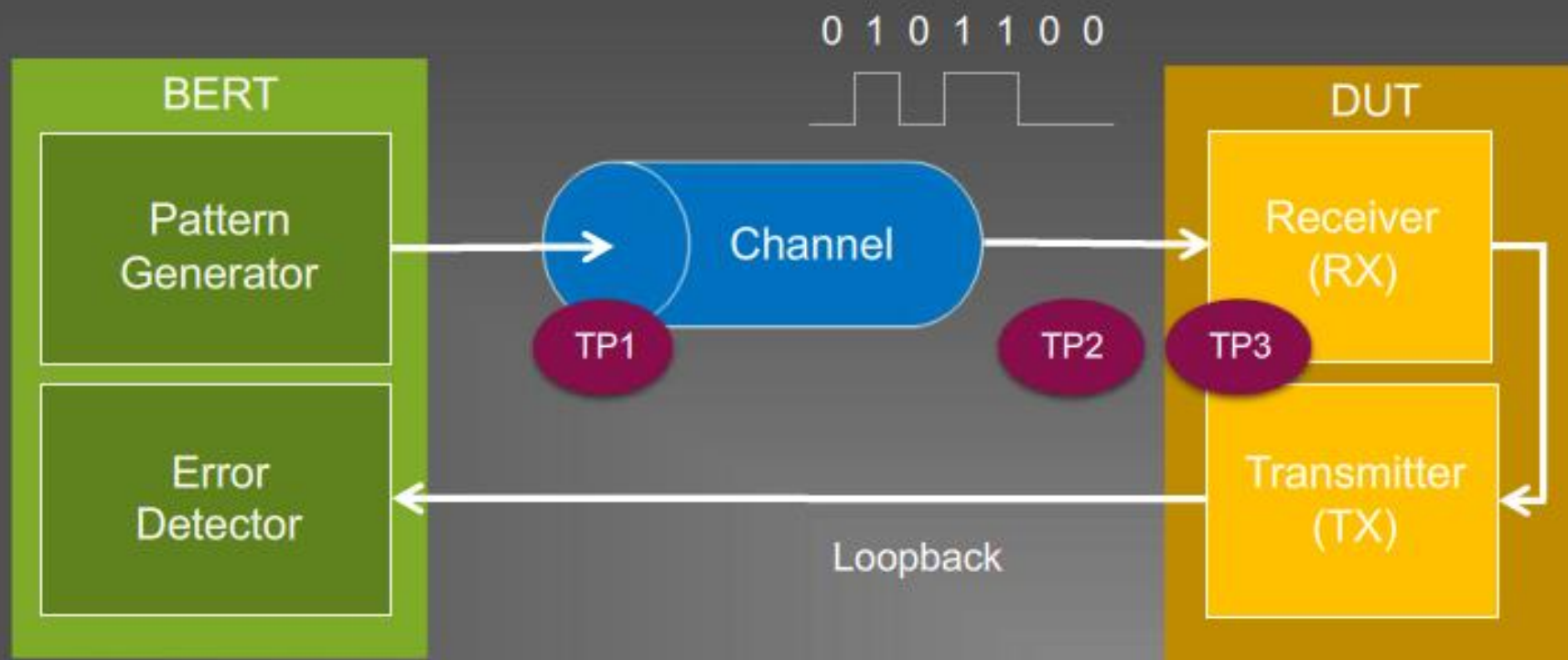
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In-situ Calibration for Accurate and Repeatable Results



- Calibration test point (TP) moves closer to RX
- Compensate for the channel loss, ISI and the test setup



J-BERT M8020A Summary

Master next generation digital designs



New Receiver Test Challenges

- Bit rates > 10 Gb/s
- > 1 channel
- De-emphasis and equalization
- Device link training
- Stress conditions at test point
- Future projects & test requirements uncertain

New Capabilities of M8020A

- Streamlined test setups by higher integration
- Faster loopback with interactive link training
- Accurate results with in-situ calibration
- Scalable configurations

Benefits for R&D and Test Engineers

- Faster test setup and link training
- Accurate and repeatable results
- Scalable to fit needs & budget
- Expandable to future needs



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Thank you!

More information:

www.agilent.com/find/M8000

www.agilent.com/find/M8020A